CLAIMS

What is claimed is:

1. A method for improving charge mobility of both NMOS and PMOS devices comprising the steps of:

providing a semiconductor substrate comprising gate structures overlying respective PMOS and NMOS device regions;

forming silicides adjacent the respective gate structures and over an upper portion of the respective gate structures;

forming a first dielectric layer comprising a stress type selected from the group consisting of tensile stress and compressive stress over the respective PMOS and NMOS device regions;

removing a portion of the first dielectric layer overlying one of the PMOS and NMOS device regions;

forming a second dielectric layer comprising a stress type opposite from the first dielectric layer stress type over the respective PMOS and NMOS device regions; and,

removing a portion of the second dielectric layer overlying one of the PMOS and NMOS device regions having the underlying first dielectric layer to form a compressive stress dielectric layer over the PMOS device region and a tensile stress dielectric layer over the NMOS device region.

2. The method of claim 1, further comprising forming a buffer oxide layer over the compressive stress dielectric layer and tensile stress dielectric layer.

3. The method of claim 2, wherein the buffer oxide layer comprises a silicon oxide layer.

4. The method of claim 2, wherein the buffer oxide layer is from about 10 Angstroms to about 1000 Angstroms in thickness.

5. The method of claim 1, wherein the first and second dielectric layers comprises a material selected from the group consisting of silicon nitride and silicon oxynitride.

6. The method of claim 1, wherein the first and second dielectric layers are formed by a CVD deposition process selected from the group consisting of LPCVD, ALCVD, and PECVD.

7. The method of claim 6, wherein the first and second dielectric layers are formed by precursors comprising reactants selected from the group consisting of silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8), dichlorosilane (SiH_2Cl_2), trichlorosilane ($SiHCl_3$), hexacholorodisilane (Si_2Cl_6), and mixtures thereof.

8. The method of claim 1, wherein the first and second dielectric layers are from about 10 Angstroms to about 1000 Angstroms in thickness.

9. The method of claim 1, wherein the compressive stress dielectric layer and the tensile stress dielectric layer comprise a stress level up to about 2 GPa.

10. The method of claim 1, wherein the silicide comprises a metal silicide.

11. The method of claim 10 wherein the metal silicide is selected from the group consisting of cobalt silicide and titanium silicide.

12. The method of claim 1, wherein the first and second dielectric layers are formed without a subsequent ion implantation process to relieve a stress level.

13. The method of claim 1, wherein the first and second dielectric layers form a contact etching stop layer in a subsequent damascene formation process.

14. A method for simultaneously improving charge mobility and device drive current of NMOS and PMOS devices comprising the steps of:

providing a semiconductor substrate comprising gate structures and offset spacers overlying respective PMOS and NMOS device regions;

forming source/drain regions;

forming silicides over the source/drain regions and over an upper portion of the respective gate structures;

forming a first dielectric layer comprising a stress type selected from the group consisting of tensile stress and compressive stress over the respective PMOS and NMOS device regions;

removing a portion of the first dielectric layer overlying one of the PMOS and NMOS device regions;

forming a second dielectric layer comprising a stress type opposite from the first dielectric layer stress type over the respective PMOS and NMOS device regions; and,

removing the second dielectric layer overlying one of the PMOS and NMOS device regions to form a compressive stress dielectric layer over the PMOS device region and a tensile stress dielectric layer over the NMOS device region.

15. The method of claim 14, further comprising forming a buffer oxide layer over the compressive stress dielectric layer and tensile stress dielectric layer.

16. The method of claim 15, wherein the buffer oxide layer comprises a silicon oxide layer.

17. The method of claim 15, wherein the buffer oxide layer is from about 10 Angstroms to about 1000 Angstroms in thickness.

18. The method of claim 14, wherein the first and second dielectric layers comprise a material selected from the group consisting of silicon nitride and silicon oxynitride.

19. The method of claim 14, wherein the first and second dielectric layers are formed by a CVD deposition process selected from the group consisting of LPCVD, ALCVD, and PECVD.

20. The method of claim 19, wherein the first and second dielectric layers are formed by precursors comprising a reactant selected from the group consisting of silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8), dichlorosilane (SiH_2Cl_2), trichlorosilane ($SiHCl_3$), hexacholorodisilane (Si_2Cl_6), and mixtures thereof.

21. The method of claim 14, wherein the first and second dielectric layers are from about 10 Angstroms to about 1000 Angstroms in thickness.

22. The method of claim 14, wherein the compressive stress dielectric layer and the tensile stress dielectric layer comprise a stress level up to about 2 GPa.

23. The method of claim 14, wherein the silicides comprise a metal silicide selected from the group consisting of cobalt silicide and titanium silicide.

24. The method of claim 14, wherein the first and second dielectric layers are formed without a subsequent ion implantation process to relieve a stress level.

25. The method of claim 1, wherein the first and second dielectric layers form a contact etching stop layer in a subsequent damascene formation process.

26. A semiconductor device pair comprising respective NMOS and PMOS devices with improved charge mobility comprising:

a semiconductor substrate;

PMOS and NMOS devices on the substrate each comprising a gate dielectric, a gate electrode, and dielectric offset spacers;

wherein the PMOS and NMOS devices further comprise source and drain (S/D) regions;

wherein the PMOS and NMOS devices further comprise silicides over the S/D regions and over an upper portion of the gate electrodes; and,

wherein the PMOS and NMOS devices further comprise a compressive stress dielectric layer disposed over the PMOS device and a tensile stress dielectric layer disposed over the NMOS device.

27. The semiconductor device of claim 26, further comprising a buffer oxide layer disposed over the compressive stress dielectric layer and the tensile stress dielectric layer.

28. The semiconductor device of claim 27, wherein the buffer oxide layer comprises a silicon oxide layer.

29. The semiconductor device of claim 27, wherein the buffer oxide layer is from about 10 Angstroms to about 1000 Angstroms in thickness.

30. The semiconductor device of claim 26, wherein the first and second dielectric layers comprise a material selected from the group consisting of silicon nitride and silicon oxynitride.

31. The semiconductor device of claim 26, wherein the first and second dielectric layers are from about 10 Angstroms to about 1000 Angstroms in thickness.

32. The semiconductor device of claim 26, wherein the compressive stress dielectric layer and a tensile stress dielectric layer comprise a stress level up to about 2 GPa.

33. The semiconductor device of claim 26, wherein the silicides comprise a metal silicide selected from the group consisting of cobalt silicide and titanium silicide.

34. The semiconductor device of claim 26, wherein the gate dielectric is selected from the group consisting of silicon oxide, silicon oxynitride, silicon nitride, a high permittivity dielectric, and combinations thereof.

35. The semiconductor device of claim 34, wherein the high permittivity dielectric is selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide, cerium oxide, titanium oxide, tantalum oxide, and combinations thereof.

36. The semiconductor device of claim 26, wherein the gate electrode comprises a material selected from the group consisting of polysilicon, polysilicon-germanium, metals, metal silicides, metal nitrides, metal oxides, and combinations thereof.

37. The semiconductor device of claim 26, wherein the offset spacers comprise a material selected from the group consisting of oxides, nitrides, and combinations thereof.

38. The semiconductor device of claim 26, further comprising an overlying ILD layer comprising metal filled damascenes extending through the compressive and tensile stress dielectric layers to the source/drain regions.

39. A semiconductor device comprising oppositely strained NMOS and PMOS devices to improve charge mobility comprising:

a semiconductor substrate;

PMOS and NMOS devices on the substrate each comprising a gate dielectric, a gate electrode, and dielectric offset spacers;

wherein the PMOS and NMOS devices further comprise source and drain (S/D) regions;

wherein the PMOS and NMOS devices further comprise silicides over the S/D regions and overlying an upper portion of the gate electrodes;

wherein the PMOS and NMOS devices further comprise a first dielectric layer disposed over the PMOS device and a second dielectric layer disposed over the NMOS device; and,

wherein the respective first and second dielectric layers form an interface region overlying an isolation feature disposed in the semiconductor substrate.